AMENDMENTS TO THE DRAWINGS

The attached replacement sheet of drawings includes changes to Fig. 1. Fig. 1 has been labeled "Prior Art."

REMARKS

Claims 1-7 are pending in the application. Claims 1-7 stand rejected for being written in improper form, but would be considered allowable if re-written to correct any and all informalities. Claims 1-7 are herein amended. No new matter has been entered. In light of the following remarks and claim amendments, Applicant earnestly solicits favorable reconsideration.

Specification

Figure 1 of the drawings was objected to as not containing the proper heading indicating "Prior Art". Applicant has amended Fig. 1 to show that it is "Prior Art."

The Office has objected to the title of the invention as not being descriptive. Applicant has amended the title to read "Cyclic multi-bit A/D conversion array and image sensor."

Claim Rejections - 35 U.S.C. § 112 Second Paragraph:

Claims 1-7 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to point out and distinctly claim the subject matter which the applicant regards as the invention.

Applicant has amended claims 1-7 in order to clarify the claims and address the Examiner's rejection. Applicant has provided a claim map below which corresponds to an embodiment of the claimed invention. Applicant hopes this will assist the Examiner and expedite prosecution of the application.

Amended claim 1:

An A/D conversion array comprising arrayed unit circuits, each of which comprises:

a first circuit element (3) arranged to perform A/D conversion of multiple bits per cycle;

a second circuit element (DAC) arranged to convert a digital output of said first circuit element to a resulting analogue conversion signal by first switching means (φ_{M1}, φ_{M2}, φ_{M3}) and

a first capacitor (Cl);

amplification means arranged to amplify an analogue input, the amplification means comprising a second capacitor (C2) for determining gain from a ratio of capacitance of the second capacitor (C2) and said first capacitor (Cl), the second capacitor (C2) being connectable between an input and an output of an inverting amplifier (2; 4; Al) to subtract the analogue conversion signal from the analog input;

a third circuit element arranged to sample and hold an output of said amplification means (2) by second switching means (φ_{1d}, φ_1, φ_2) and said first capacitor (C1); and

third switching means (φ_{Ad}, φ_{1d}, φ_1, φ_2) arranged to select one of the output of said amplification means and an input signal (V_{IN}) and to supply the selected signal to said amplification means (2) as input, via said first capacitor (Cl), the A/D conversion array being characterized in that:

control means arranged to control said first to third switching means is installed outside the array, and the arrayed unit circuits are arranged such that cyclic multi-bit A/D conversion is performed when the input signal (V_{IN}) is supplied as an input of said amplification means (2; 4; Al) in a first stage, and a signal from said third circuit element is supplied to the input of said amplification means in a next stage.

Amended claim 2:

The A/D conversion array according to Claim 1, wherein two first capacitors (Cl) are arranged to be used for D/A conversion with said amplification means, and a conversion speed per cycle is doubled by alternately using said two first capacitors (Cl) for D/A conversion and for sampling and holding.

Amended claim 3:

The A/D conversion array according to Claim 1, wherein said circuit element arranged to perform A/D conversion of N-bits is arranged to divide input analog signals into three voltage ranges, and to assign values 1, 0 and -1 to the three ranges.

Amended claim 4:

The A/D conversion array according to Claim 1, wherein an amplifier in said amplification means is a differential amplifier (4) having a differential input and a differential output, and a full differential circuit is structured by said differential amplifier, a capacitor and switching means.

Amended claim 5:

An image sensor, arranged to perform A/D conversion in parallel for outputs of elements of an image sensor array thereof comprising an A/D conversion array as claimed in any one of Claims 1 to 4 located in a column of the image sensor array.

Amended claim 6:

The image sensor according to Claim 5, further comprising a noise cancellation circuit in a column of said image sensor array, wherein said noise cancellation circuit comprises a noise

cancellation inverting amplifier, a first noise cancellation capacitor connected between the output of the image sensor array and the input of said noise cancellation inverting amplifier, and a second noise cancellation capacitor connected between the input and output of said noise cancellation inverting amplifier (A2), and switching means arranged such that, and the inverting amplifier (2) in said A/D conversion array is also arranged to be used as the noise cancellation inverting amplifier of said noise cancellation circuit, said first capacitor (Cl) is also arranged to be used as said first noise cancellation capacitor, and said second capacitor (C2) is also arranged to used as said second noise cancellation capacitor.

Amended claim 7:

The image sensor according to Claim 6, further comprising a fifth capacitor (C3) arranged to be connected between the output of the image sensor array and input of the inverting amplifier only during a noise cancellation operation, characterized in that an amplification function is acquired by a ratio of a sum of the capacitance of the first capacitor (Cl) and the third capacitor (C3) with said second capacitor (C2).

In view of the aforementioned amendments and accompanying remarks, Applicant submits that that the claims, as herein amended, are in condition for allowance. Applicant requests such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned agent to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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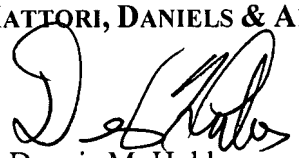

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SGA/DMH/klf
Attachment: Replacement Fig. 1